IN THE CLAIMS:

1. (Currently Amended) A method of designing a circuit layout of a semiconductor integrated circuit, comprising:

designing a logic function of the integrated circuit;

designing a pattern layout of the integrated circuit so that the pattern layout includes a logic cell area and an open area;

providing a spare underground cell having no interconnect patterns and contacts;

inserting said spare underground cell into the open area, wherein the spare underground cell includes a functional element; and

designing a mask layout of the integrated circuit, the mask layout including the logic cell and the spare underground cell;

wherein the inserting the spare underground cell into the distributed open area comprises:

pointing out an open area in an attended block region and an attended spare underground cell;

inserting the attended spare underground cell into the open area in the attended block region;

renewing the attended block region; and

setting a flag when all inserting within the attended block region are finished.

2. (Previously Presented) The method of designing the circuit layout according to claim 1, wherein the functional element comprises a D flip-flop, an inverter, a NOR circuit, and NAND circuit, an exclusive OR circuit and a latch circuit.

3. (Previously Presented) The method of designing the circuit layout according to claim 1, wherein inserting the spare underground cell comprises:

dividing the pattern layout into a plurality of block regions;

searching the open area from the block regions;

distributing the open area into the block regions; and

inserting the spare underground cell into the distributed open area.

4. (Cancelled)

5. (Currently Amended) The method of designing the circuit layout according to claim [[4]] 1, wherein the inserting the spare underground cell into the distributed open [[are]] area further comprises:

renewing the attended spare underground cell; and

repeating the pointing out, the inserting the attended spare underground cell with another open area in another attended block region and another attended spare underground cell until all of the block regions are finished.

6. (Withdrawn) A method of changing a circuit layout of a semiconductor integrated circuit, comprising:

preparing the circuit layout including a logic cell area and a spare underground cell area, wherein the spare underground cell area has no interconnect patterns and contacts and includes a functional element;

hypothetically disposing a changing layout into the spare underground cell area;

preparing a list of the changing layout;

deciding the position of the changing layout; and

automatically setting a conductive pattern layout of the semiconductor integrated circuit.

7. (Withdrawn) The method of changing the circuit layout according to claim 6, wherein the functional element comprises a D flip-flop, an inverter, a NOR circuit, a NAND circuit, an exclusive OR circuit and a latch circuit.

8. (Withdrawn) The method of changing the circuit layout according to claim 6, wherein the disposing comprises:

deleting a logic cell to be changed; and

adding a spare underground cell for replacing the deleted logic cell in the spare underground cell area.

9. (Withdrawn) The method of changing the circuit layout according to claim 6, further comprising designing a mask of the semiconductor integrated circuit after the setting.

10. (Currently Amended) A method of designing a circuit layout of a semiconductor integrated circuit, comprising:

designing a logic function of the integrated circuit;

designing a pattern layout of the integrated circuit so as to include a plurality of logic cells in a logic cell area and an open area;

providing a plurality of spare underground cells having no interconnect patterns and contacts;

inserting said plurality of spare underground cells into the open area, wherein each of the spare underground cells includes a plurality of functional elements; and

designing a mask layout of the integrated circuit, the mask layout including the logic cells and the spare underground cells,

wherein the inserting the spare underground cells into the distributed open area comprises:

pointing out an open area in an attended block region and an attended spare underground cell;

inserting the attended spare underground cell into the open area in the attended block region;

renewing the attended block region; and

setting a flag when all inserting within the attended block region are finished.

11. (Previously Presented) The method of designing the circuit layout according to claim 10, wherein the functional elements includes a D flip-flop, an inverter, a NOR circuit, a NAND circuit, an exclusive OR circuit and a latch circuit.

12. (Previously Presented) The method of designing the circuit layout according to claim 10, wherein each of the spare underground cells has a same kind of the functional elements.

13. (Previously Presented) The method of designing the circuit layout according to claim 10, wherein inserting the spare underground cells comprises:

dividing the pattern layout into a plurality of block regions;

searching the open area from the block regions;

distributing the open area into the block regions; and

inserting the spare underground cells into the distributed open area.

14. (Cancelled)

15. (Currently Amended) The method of designing the circuit layout according to claim [[14]] 10, wherein the inserting the spare underground cells into the distributed open area further comprises:

renewing the attended spare underground cell; and

repeating the pointing out, the inserting the attended spare underground cell, renewing the attended block region, setting and renewing the attended spare underground cell with another open area in another attended block region and another attended spare underground cell until all of the block regions are finished.